Please amend the specification as follows:

In the Claims:

~~18~~ 1. (amended) An apparatus comprising a semiconductor device which includes:

laterally spaced first and second sections with respective upwardly facing first and second surface portions thereon;

a third section projecting upwardly beyond each of said first and second surface portions from a location therebetween, said third section having two side surfaces on opposite sides thereof;

a substantially planar insulating layer which has portions disposed over said first and second surface portions, said third section extending into said insulating layer, and said insulating layer having first and second recess portions which respectively extend downwardly through said insulating layer toward said first and second surface portions on opposite sides of said third section, each said recess portion being immediately adjacent a respective said side surface of said third section;

a first portion of conductive material disposed in said first recess portion; and

a second portion of conductive material disposed in said second recess portion.

Please add the following new claims:

14 ~~31~~. The apparatus of Claim ~~18~~ 1, wherein said side surfaces of said third section comprise an insulator, said insulator different from said substantially planar insulating layer.

15 ~~32~~. The apparatus of Claim ~~31~~ 14, wherein said insulator is nitride and said substantially planar insulating layer is oxide.

16
~~33~~. The apparatus of Claim ~~23~~, further comprising a substantially planar insulating layer coplanar with said insulating layer covering said top portion of said control terminal, wherein said control terminal and said first and second terminals are within an opening in said substantially planar insulating layer.

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~~34~~. The apparatus of Claim ~~33~~, wherein said insulating layer covering said side portions and said top portion of said control terminal is nitride and said substantially planar insulating layer is oxide.

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18 18
~~35~~. The integrated circuit of Claim ~~27~~, further comprising a substantially planar insulating layer coplanar with said insulating material covering said side and top portions of said gate stack, wherein said gate stack and said local interconnection terminals are within an opening in said substantially planar insulating layer.

19 18
~~36~~. The apparatus of Claim ~~35~~, wherein said insulating layer material covering said side and top portions of said gate stack is nitride and said substantially planar insulating layer is oxide.

REMARKS

Reconsideration of the above-referenced application in view of the amendments and the following remarks is respectfully requested.

The Office Action indicates that only Claims 18-22 were pending in this application. However, Applicant submitted a Preliminary Amendment at the time of filing of the instant application in which Claims 23-30 were added. A copy of the Preliminary Amendment, as well as copies of the returned postcard and

18. An apparatus comprising a semiconductor device which includes:

laterally spaced first and second sections with respective upwardly facing first and second surface portions thereon;

a third section projecting upwardly beyond each of said first and second surface portions from a location therebetween, said third section having two side surfaces on opposite sides thereof;

an insulating layer which has portions disposed over said first and second surface portions, said third section extending into said insulating layer, and said insulating layer having first and second recess portions which respectively extend downwardly through said insulating layer toward said first and second surface portions on opposite sides of said third section, each said recess portion being immediately adjacent a respective said side surface of said third section;

a first portion of conductive material disposed in said first recess portion; and

a second portion of conductive material disposed in said second recess portion.

~~19.~~ 2 An apparatus according to Claim ~~18~~ 1, including a semiconductor substrate having spaced source and drain regions which serve as said first and second sections, and including between said source and drain regions a gate section which includes a gate dielectric layer, a gate electrode over said gate dielectric layer, an insulator layer over said gate electrode, and insulator sidewalls on opposite sides of said gate dielectric layer, said gate electrode, and said insulator layer, wherein said gate section is said third section.

20. An apparatus according to Claim 19, wherein said first and second portions of conductive material have respective upwardly facing third and fourth surface portions thereon, said third and fourth surface portions being substantially coplanar with a top surface of said insulator layer.

21. An apparatus according to Claim 19, wherein said insulator layer includes alternating layers of a nitride and an oxide.

22. An apparatus according to Claim 18, wherein said side surfaces are spaced by a distance which corresponds to a minimum gate length in said semiconductor device.

Please add the following new claims:

--23. An integrated circuit including a transistor, said transistor comprising:

a control terminal extending above a plane of semiconductor material, said control terminal having two side portions and a top portion covered by an insulating layer; and

first and second terminals on either side of said control terminal, said first and second terminals extending above said plane of semiconductor material such that top portions of said first and second terminals are substantially coplanar with said insulating layer covering said top portion of said control terminal.

24. The circuit of Claim 23, wherein said insulating layer covering said top portion of said control terminal comprises alternating sub-layers of first and second insulating materials.

25. The circuit of Claim 24, wherein said first insulating material is silicon oxide and said second insulating material is silicon nitride.

26. The circuit of Claim 23, wherein said control terminal is a gate electrode of a field effect transistor and said first and second terminals comprise local interconnections to drain and source regions of said transistor.

27. An integrated circuit including a transistor, said transistor comprising:

a gate stack extending above a plane of semiconductor material, said gate stack comprising a gate dielectric and a gate electrode over said gate dielectric, said gate electrode comprising side and top portions covered by insulating material; and

local interconnection terminals on opposing sides of said gate stack and abutting said insulating material on said side portions of said gate electrode, said local interconnection terminals extending above said plane of semiconductor

material such that top portions of said local interconnection terminals are substantially coplanar with said insulating material covering said top portion of said gate electrode.

28. The circuit of Claim 27, wherein said insulating material covering said top portion of said control terminal comprises alternating layers of first and second insulating materials.

29. The circuit of Claim 28, wherein said first insulating material is silicon oxide and said second insulating material is silicon nitride.

30. The circuit of Claim 27, wherein each of said local interconnection terminals includes a column of insulating material. –

Claims 18-30 are now pending in this Application. Applicant respectfully requests entry and consideration of these claims.

If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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